

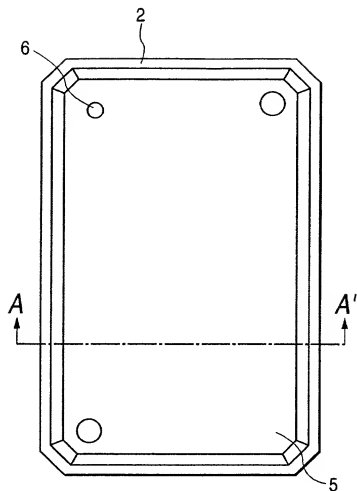
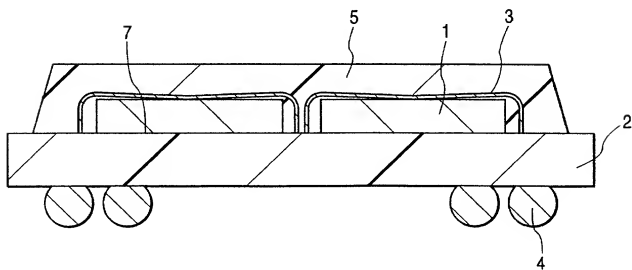
**FIG. 1****FIG. 3**

FIG. 2(a)

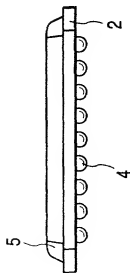


FIG. 2(b)

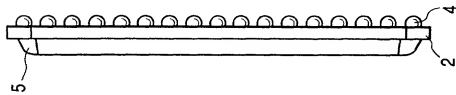


FIG. 2(c)

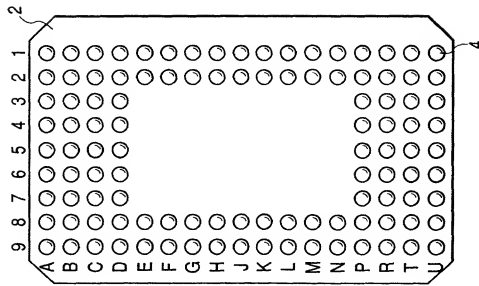


FIG. 4

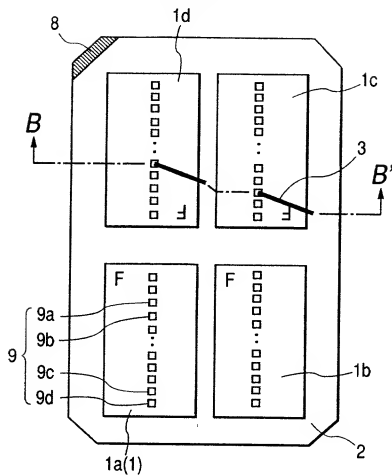


FIG. 5

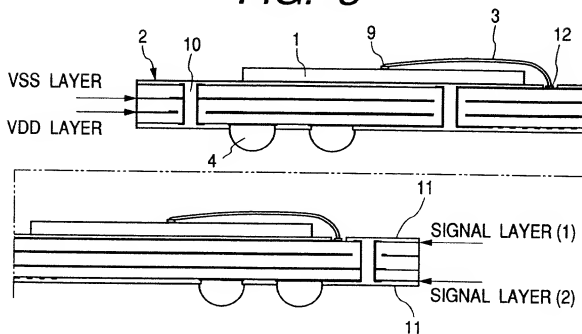
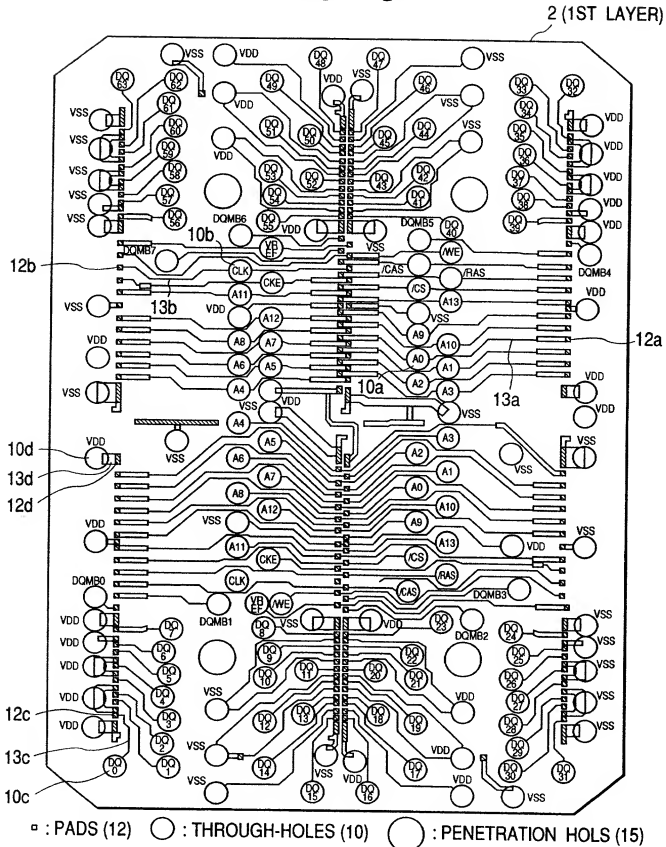
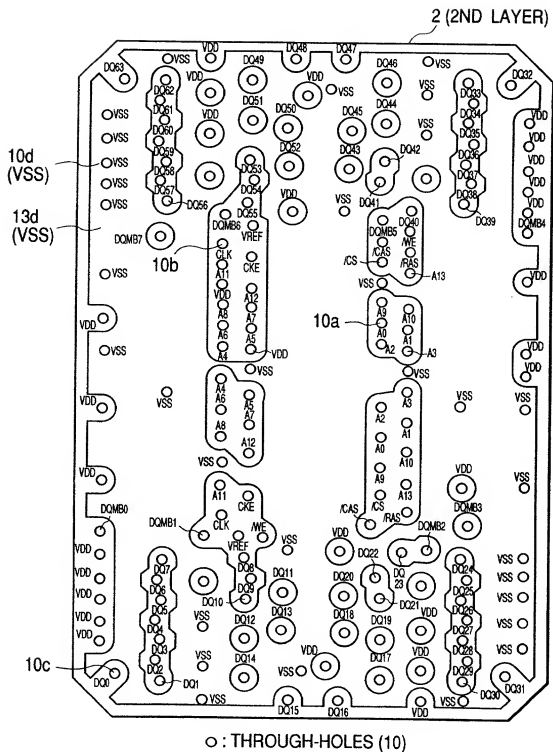


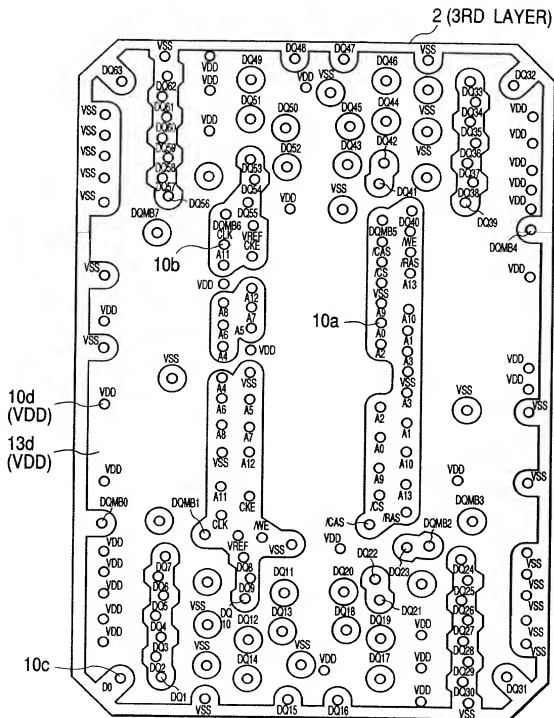
FIG. 6



2 (2ND LAYER)



○ : THROUGH-HOLES (10)



2 (4TH LAYER)

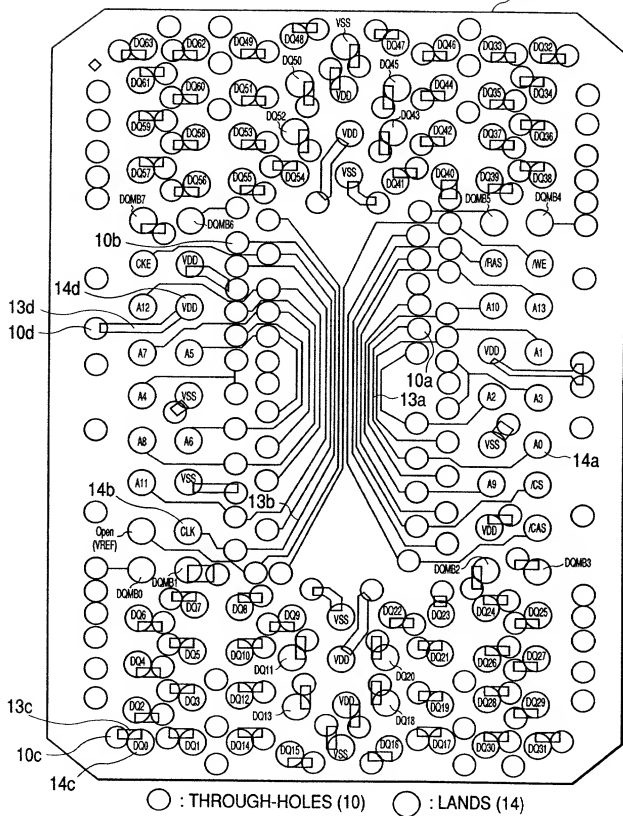


FIG. 10

2 (1ST &amp; 4TH LAYERS)

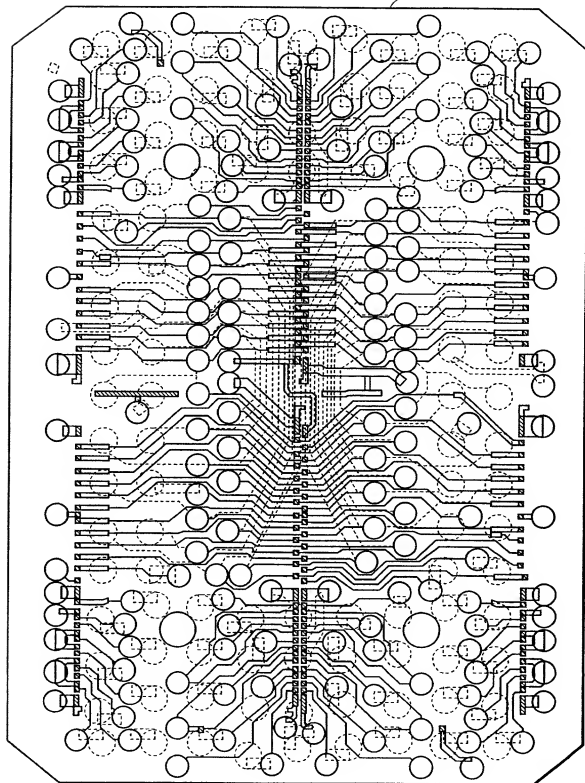




FIG. 11

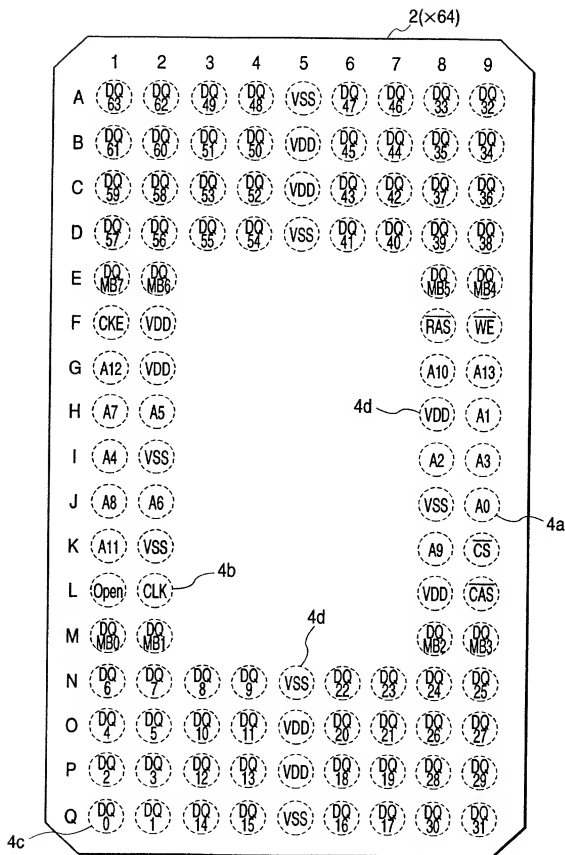


FIG. 12

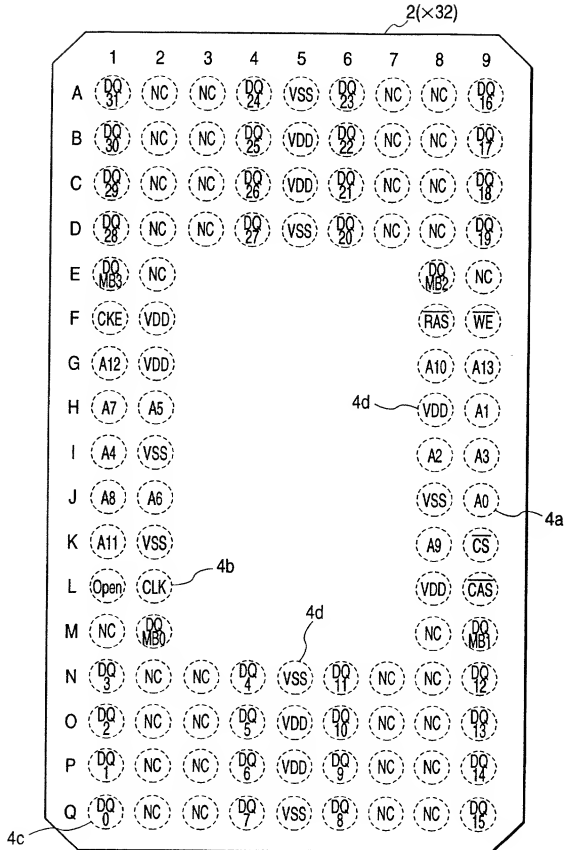


FIG. 13

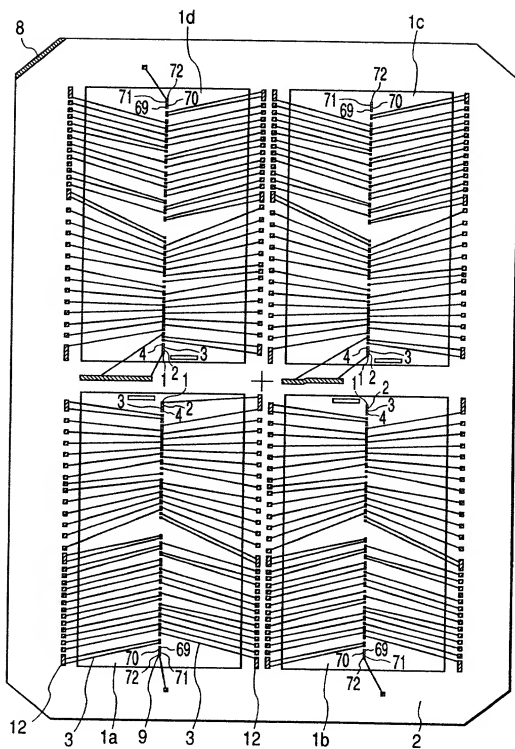


FIG. 14

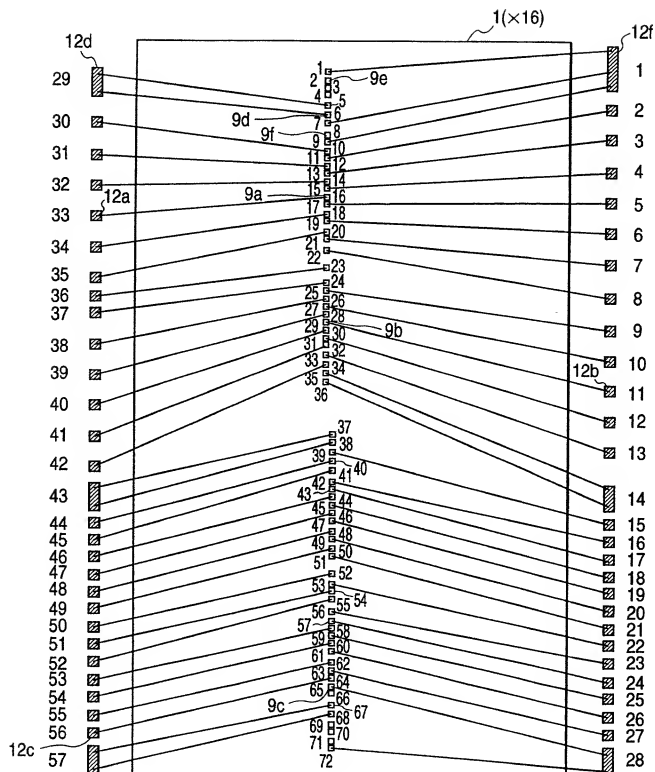


FIG. 15

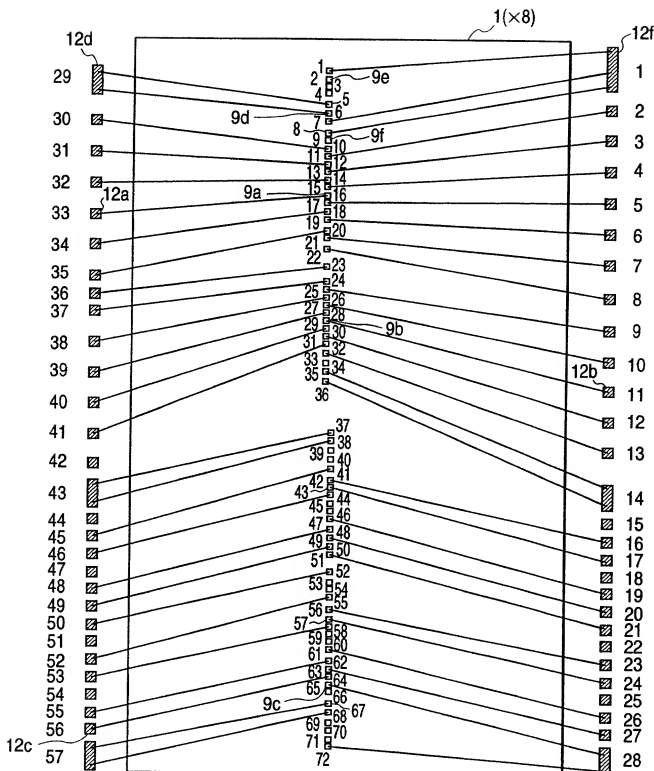


FIG. 16

PAD NO.	PAD NAMES	USE
1	VSSI	POWER SUPPLY
2	VBB	P-TEST
3	VPLT	P-TEST
4	VPP	P-TEST
5	VDDI	POWER SUPPLY
6	VDD	POWER SUPPLY
7	VSS	POWER SUPPLY
8	BOP1B	BONDING OPTION
9	BOP2B	BONDING OPTION
10	A3	INPUT (ADDRESS)
11	A4	INPUT (ADDRESS)
12	A2	INPUT (ADDRESS)
13	A5	INPUT (ADDRESS)
14	A1	INPUT (ADDRESS)
15	A6	INPUT (ADDRESS)
16	A0	INPUT (ADDRESS)
17	A7	INPUT (ADDRESS)
18	A10	INPUT (ADDRESS)
19	A8	INPUT (ADDRESS)
20	A12	INPUT (ADDRESS)
21	A9	INPUT (ADDRESS)
22	VSS	POWER SUPPLY
23	VDD	POWER SUPPLY
24	A13	INPUT (ADDRESS)
25	A11	INPUT (ADDRESS)
26	/CS	INPUT (CONTROL)
27	CKE	INPUT (CONTROL)
28	/RAS	INPUT (CONTROL)
29	CLK	INPUT (CONTROL)
30	/CAS	INPUT (CONTROL)
31	DQMU	INPUT (CONTROL)
32	/WE	INPUT (CONTROL)
33	VREF	INPUT (CONTROL)
34	DQML	INPUT (CONTROL)
35	VSSI	POWER SUPPLY
36	VSS	POWER SUPPLY
		CHIP CENTER

PAD NO.	PAD NAMES	USE
37	VDD	POWER SUPPLY
38	VDDI	POWER SUPPLY
39	DQ8	I/O DATA
40	DQ7	I/O DATA
41	VDDQ	POWER SUPPLY
42	VSSQ	POWER SUPPLY
43	DQ9	I/O DATA
44	DQ6	I/O DATA
45	DQ10	I/O DATA
46	DQ5	I/O DATA
47	VSSQ	POWER SUPPLY
48	VDDQ	POWER SUPPLY
49	DQ11	I/O DATA
50	DQ4	I/O DATA
51	VSS	POWER SUPPLY
52	VDD	POWER SUPPLY
53	DQ12	I/O DATA
54	DQ3	I/O DATA
55	VDDQ	POWER SUPPLY
56	VSSQ	POWER SUPPLY
57	DQ13	I/O DATA
58	DQ2	I/O DATA
59	DQ14	I/O DATA
60	DQ1	I/O DATA
61	VSSQ	POWER SUPPLY
62	VDDQ	POWER SUPPLY
63	DQ15	I/O DATA
64	DQ0	I/O DATA
65	VSS	POWER SUPPLY
66	BOP0B	BONDING OPTION
67	VDD	POWER SUPPLY
68	VDDIU	POWER SUPPLY
69	VPERI	P-TEST
70	VDL	P-TEST
71	VBLR	P-TEST
72	VSSIU	POWER SUPPLY
		CHIP CENTER

FIG. 17

SUBSTRATE PAD NO.	CHIP	
	PAD NAMES	
1	×16	×8
	VSS	VSS
	VSS	VSS
	BOP2B	—
2	—	BOP1B
3	A4	A4
4	A5	A5
5	A6	A6
6	A7	A7
7	A8	A8
8	A12	A12
9	VSS	VSS
10	A11	A11
11	CKE	CKE
12	CLK	CLK
13	/WE	/WE
14	VREF	VREF
15	VSS	VSS
16	VSS	VSS
17	DQ8	—
18	VSS	VSS
19	DQ9	DQ4
20	DQ10	—
21	VSS	VSS
22	DQ12	—
23	VSS	VSS
24	DQ13	DQ6
25	DQ14	—
26	VSS	VSS
27	DQ15	DQ7
28	VSS	VSS
	VSS	VSS

SUBSTRATE PAD NO.	CHIP	
	PAD NAMES	
29	×16	×8
	VDD	VDD
30	VDD	VDD
31	A3	A3
32	A2	A2
33	A1	A1
34	A0	A0
35	A10	A10
36	A9	A9
37	VDD	VDD
38	A13	A13
39	/CS	/CS
40	/RAS	/RAS
41	/CAS	/CAS
42	DQMU	DQM
43	DQML	—
44	VDD	VDD
45	VDD	VDD
46	DQ7	—
47	VDD	VDD
48	DQ6	DQ3
49	DQ5	—
50	VDD	VDD
51	VDD	VDD
52	DQ3	—
53	VDD	VDD
54	DQ2	DQ1
55	DQ1	—
56	VDD	VDD
57	DQ0	DQ0
	VDD	VDD
	VDD	VDD

— : NC

FIG. 18

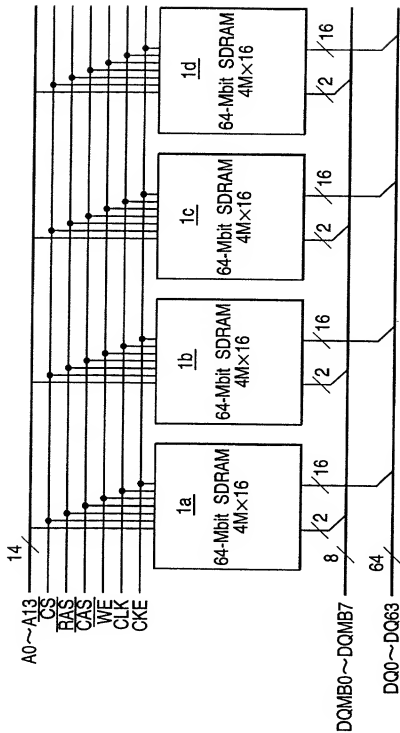




FIG. 19

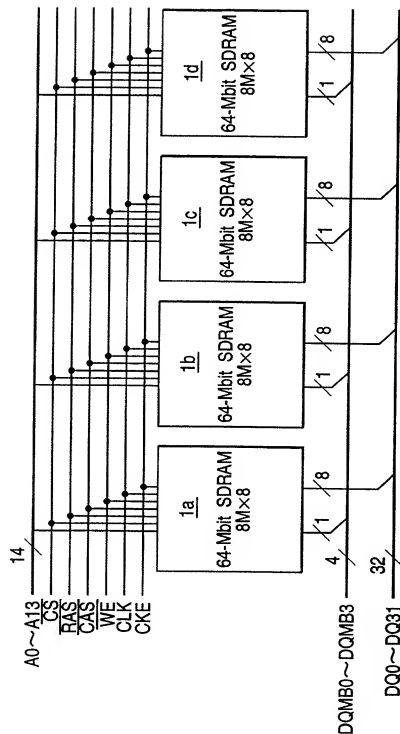


FIG. 20

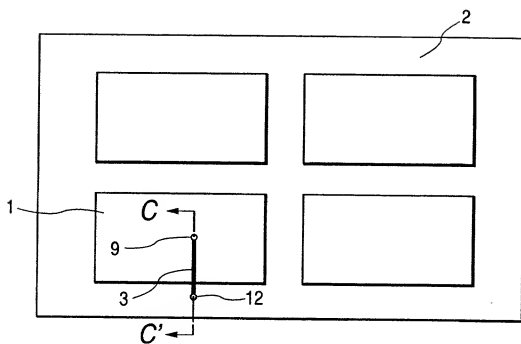
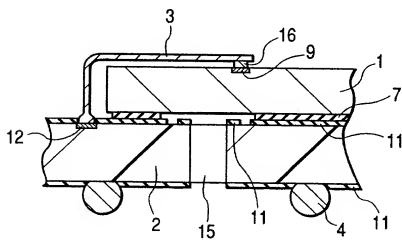


FIG. 21



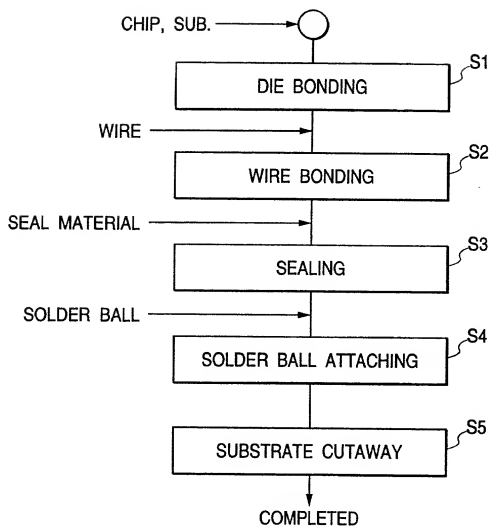
**FIG. 22**

FIG. 23

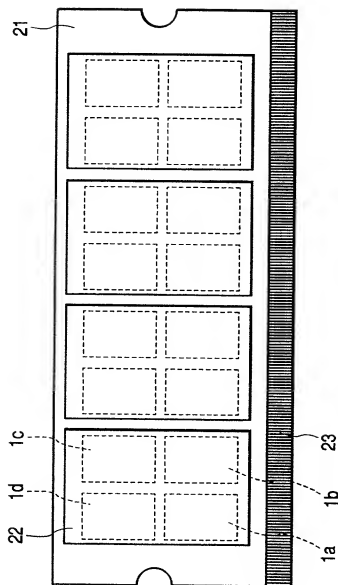


FIG. 24

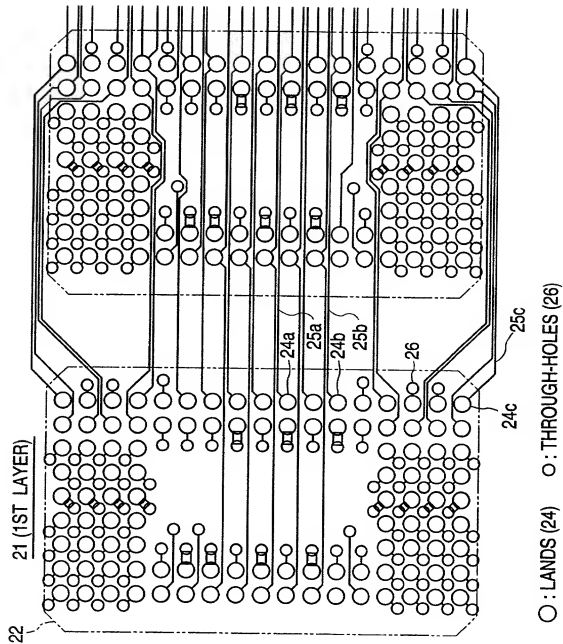


FIG. 25

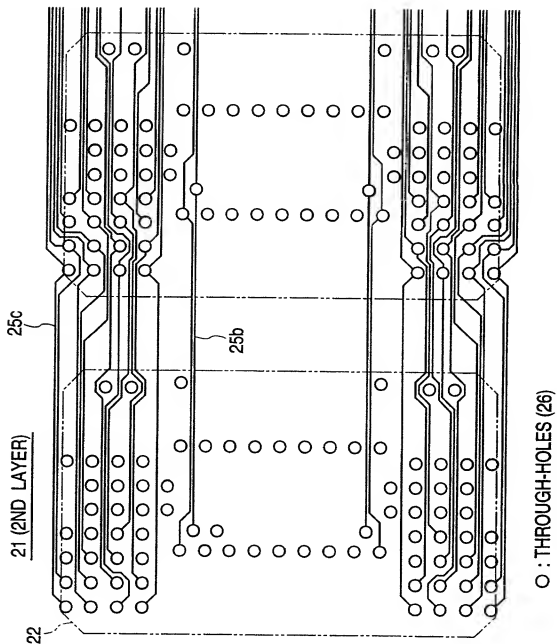


FIG. 26

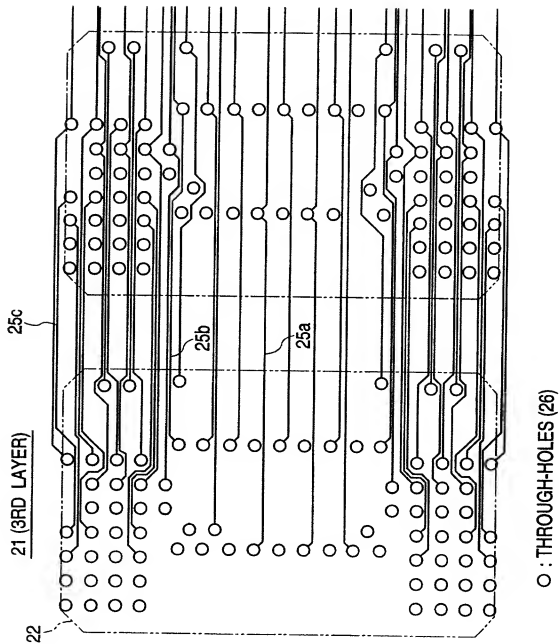


FIG. 27

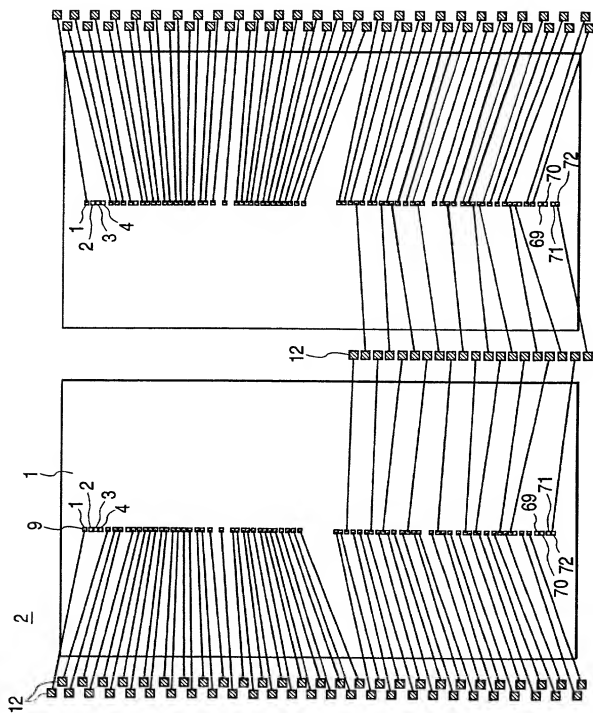




FIG. 28

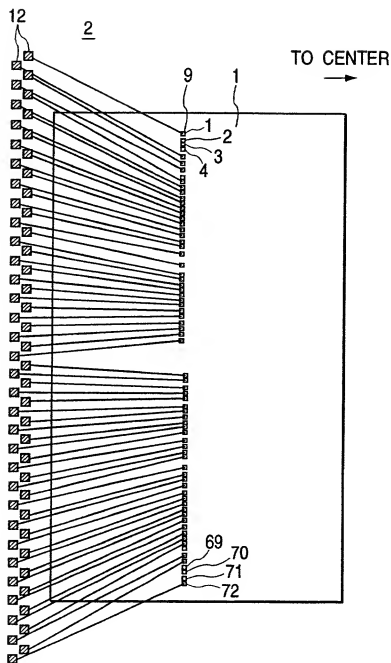


FIG. 29

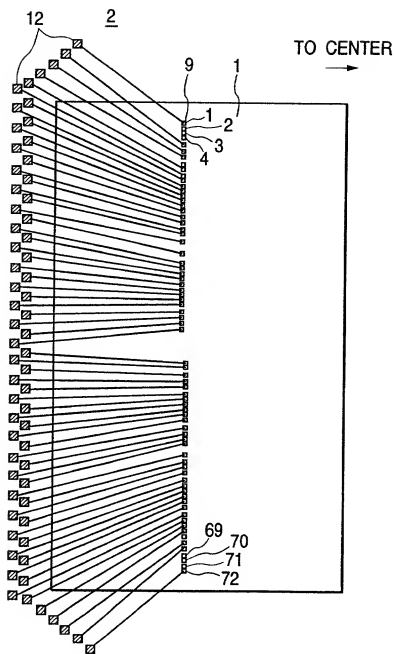


FIG. 30

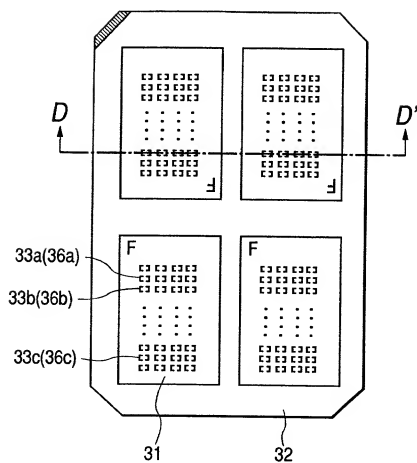


FIG. 31

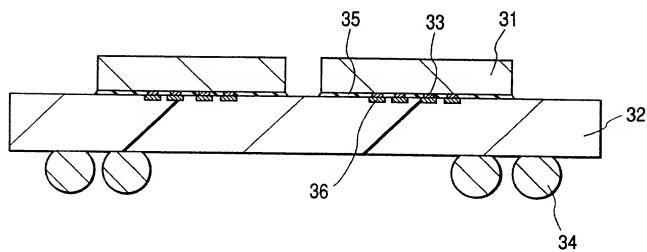


FIG. 32

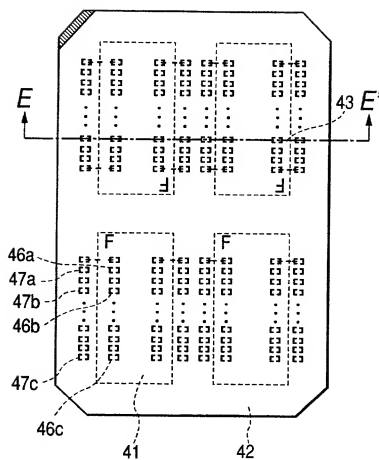


FIG. 33

